CLAIMS

We claim:

1. An apparatus comprising:

a data aligner to receive data from a data transmission link and to align the data into predefined segments for interim storage; and

a buffer to receive aligned data from the data aligner for interim storage and to reassemble data output onto a wider data path, the buffer to allow storage of aligned data in wider format to maintain sufficient bandwidth to account for frequency scaling of received data rate to frequency of the data path and fragmentation of data for alignment onto the data path, but in which the buffer to use multiple memory storage devices having a single read port and a single write port to write data of predefined segments from the data aligner.

2. The apparatus of claim 1, wherein the buffer is arranged in arrays formed from the multiple memory storage devices.

3. The apparatus of claim 2 further including a command control logic to separate commands from data at an input to the data aligner and to process commands to align the data.

4. The apparatus of claim 3 further comprises a data re-aligner at the buffer output, wherein the buffer includes a number of arrays in which data entry may start in any one of the arrays and an orientation bit or bits is to be used to identify the starting array for re-alignment in the data re-aligner.

5. The apparatus of claim 4 further including a meta-data unit to receive meta-data from the command control logic and to use the meta-data to realign the data in the data re-aligner.

6. The apparatus of claim 5 further comprising a data fragment collector to collect fragments of data that do not fit into the predefined segment in one clock period and to use the fragment in a next clock period to fit into a next segment.

7. The apparatus of claim 4 wherein the received data is based on SPI-4 protocol.

8. The apparatus of claim 4 wherein the received data is based on HyperTranspot protocol.

9. An integrated circuit comprising:

an interface unit to receive incoming data from a higher frequency data transmission link for use by the integrated circuit;

a command control unit to receive incoming data from the interface unit and to separate commands from data to process commands to align the data;

a data aligner to receive incoming data from the interface unit and to align the incoming data into a predefined segment for interim storage; and

a reassembly buffer to receive aligned data from the data aligner for interim storage and to reassemble data output onto an internal data path, the reassembly buffer to allow storage of aligned data in wider format to maintain sufficient bandwidth to account for frequency scaling of received data rate to frequency of the internal data path and fragmentation of data for alignment onto the internal data path, but in which the reassembly buffer to use multiple memory storage devices having a single read port and a single write port to write data of predefined segments from the data aligner.

10. The integrated circuit of claim 9, wherein the reassembly buffer is arranged in arrays formed from the multiple memory storage devices.

11. The integrated circuit of claim 9, wherein the reassembly buffer is structured having multiple matrices arranged into arrays, in which a width of the individual matrix is determined by the internal data path.

12. The integrated circuit of claim 10 further comprises a data re-aligner at the reassembly buffer output, wherein an orientation bit or bits is generated at the data aligner and sent to the data re-aligner to be used to identify the starting array for re-alignment in the data re-aligner.

13. The integrated circuit of claim 12 further including a meta-data unit to receive meta-data from the command control logic and to use the meta-data to realign the data in the data re-aligner.

14. The integrated circuit of claim 13 further comprising a data fragment collector to collect fragments of data that do not fit into the predefined segment in one clock period and to use the fragment in a next clock period to fit into a next segment.

15. The integrated circuit of claim 14 wherein one input decode and routing unit decodes and routes incoming data based on SPI-4 protocol.

16. The integrated circuit of claim 14 wherein one input decode and routing unit decodes and routes incoming data based on HyperTransport protocol.

17. A method comprising:

aligning data received from a data transmission link into predefined segments for interim storage; and

buffering aligned data in a buffer for interim storage and to reassemble data output data onto an internal data path of an integrated circuit, the buffering to allow storage of aligned data in wider format to maintain sufficient bandwidth to account for frequency scaling of received data rate to frequency of the internal data path and fragmentation of data for alignment onto the internal data path, but the buffering is achieved through buffer arrays in which individual array elements uses single read port and a single write port to write data of predefined segments from the aligner.

18. The method of claim 17, wherein the buffering is achieved by use of multiple memory storage devices.

19. The method of claim 18 wherein the buffering allows a data entry to start in any one of the arrays and an orientation bit or bits is used to identify the starting array for aligning and subsequent re-aligning at the output of the buffer.

20. The method of claim 19 wherein the data is based on SPI-4 protocol.

21. The method of claim 19 wherein the data is based on HyperTransport protocol.